



COPY OF PAPERS
ORIGINALLY FILED

RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2811
PATENT APPLICATION
Do. No. 5484-53

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Tae-Gyoung KANG

Serial No. 09/458,506

Examiner: Nadav, Ori

Filed: December 9, 1999

Group Art Unit: 2811

For: LAYOUT METHOD OF SEMICONDUCTOR DEVICE

BOX AF
Assistant Commissioner for Patents
Washington, D.C. 20231

TECHNOLOGY CENTER 2800

FEB 25 2002

8/B (X)
FJONES
2027-02
RECEIVED

AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR 1.116

Responsive to the Final Office Action, dated November 21, 2001, please amend the application as follows.

IN THE SPECIFICATION

On page 5, following the brief description of Fig. 16 (which we added in our Response to the Office Action dated March 28, 2001) please further add:

Fig. 17 illustrates a power voltage applying line and a grounding voltage applying line.

IN THE CLAIMS

Please amend the claims as follows:

14. (Amended) A semiconductor device comprising:
- a substrate;
 - active regions of two or more adjacent transistors, the active regions having at least more than one first and second electrodes disposed on the substrate;
 - a plurality of transistor gates disposed on the substrate between more than one first and second electrodes of those active regions respectively, wherein two or more gates are of a predetermined width and length at a substantially identical gap between ones of the adjacent transistor gates, without intervening transistor gates therebetween, on the substrate; and
 - a plurality of dummy gates having predetermined width and length between ones of the adjacent transistors at a substantially identical gap between adjacent ones of the dummy

do not
enr
on
B1
sub
CI



Corres. and Mail
COPY OF PAPERS
ORIGINAL FILED
BOX AF

AF/280
RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2811
PATENT APPLICATION
Do. No. 5484-53

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Tae-Gyoung KANG

Serial No. 09/458,506

Examiner: Nadav, Ori

Filed: December 9, 1999

Group Art Unit: 2811

For: LAYOUT METHOD OF SEMICONDUCTOR DEVICE

BOX AF

Assistant Commissioner for Patents
Washington, D.C. 20231

RECEIVED
FEB 25 2002
TECHNOLOGY CENTER 2800

Responsive to the Final Office Action dated November 21, 2001, enclosed is an amendment in the above-identified application.

The fee has been calculated as shown below.

CLAIMS AS AMENDED					
For:	Number After Amendment	Previous Number	Extra	Rate	Additional Fee
Total Claims	23	-23	0	x \$18 =	\$0
Independent Claims	6	-6	0	x \$80 =	\$0
TOTAL ADDITIONAL FEE FOR THIS AMENDMENT					\$0

*greater of twenty (20) or number for which fee has been paid

**greater of three (3) or number for which fee has been paid

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



20575

PATENT TRADEMARK OFFICE

Alan T. McCollom
Reg. No. 28,881

MARGER JOHNSON & McCOLLOM, P.C.
1030 SW Morrison Street
Portland, OR 97205
(503) 222-3613

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO:
[] COMMISSIONER OF PATENTS AND TRADEMARKS, WASHINGTON D.C. 20231
[x] ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON D.C. 20231
[] ASSISTANT COMMISSIONER FOR TRADEMARKS, 2900 CRYSTAL DRIVE, ARLINGTON VA 22202-3513
ON 1-22-02